Electronic Version
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Claims

[c1] A method of accessing a storage cell of a dynamic random access memory (DRAM) having an array of gain cells being read accessible by a read wordline and a read bitline, and being write accessible by a write wordline and write bitline separate from said read wordline and read bitline, comprising:
activating a read wordline of said array of gain cells to permit signals from a plurality of gain cells coupled to said read wordline to develop on a plurality of corresponding read bitlines coupled to said plurality of gain cells;
generating an interlock signal in said DRAM after activating said read wordline; and
deactivating said read wordline in response to said interlock signal.

[c2] The method of claim 1 further comprising timing the precharging of read bitlines of said array of gain cells in relation to said interlock signal.

[c3] The method of claim 1 further comprising timing the setting of sense amplifiers coupled to read bitlines of said array of gain cells in relation to said interlock signal.

[c4] The method of claim 1 further comprising setting sense amplifiers to amplify signals on said read bitlines in response to said interlock signal.

[c5] The method of claim 1 wherein said interlock signal is generated in response to a change in voltage of a sample bitline of said DRAM, said sample bitline being coupled to a plurality of gain cells and a sample sense amplifier.

[c6] The method of claim 5 wherein said interlock signal is generated by differentially amplifying a difference in the voltage of said sample bitline relative to a reference voltage.

[c7] The method of claim 6 further comprising programmably adjusting a level of said reference voltage to adjust triggering of said interlock signal.

[c8] The method of claim 7 wherein said reference voltage level is adjusted relative to an operating condition of said DRAM including at least one selected from the group consisting of temperature and supply voltage.

[c9] The method of claim 7 wherein said reference voltage level is adjusted relative to a retention time of said DRAM.

[c10] The method of claim 5 wherein said voltage of said sam-

ple bitline changes in response to accessing a gain cell of said plurality of gain cells coupled thereto, said gain cell having a three transistor, one capacitor structure.

[c11] A dynamic random access memory (DRAM), comprising:
an array of gain cells being read accessible by a read wordline and a read bitline, and being write accessible by a write wordline and write bitline separate from said read wordline and said read bitline;
a row decoder operable in response to a row address strobe signal to activate a read wordline of said array of gain cells to permit signals from a plurality of gain cells coupled to said read wordline to develop on a plurality of corresponding read bitlines coupled to said plurality of gain cells; and
a circuit operable to generate an interlock signal at a time after said row address strobe signal,
wherein said row decoder is further operable to deactivate said read wordline in response to said interlock signal.

[c12] The DRAM of claim 11 further including sense amplifiers, operable to amplify signals on bitlines connected thereto in response to said interlock signal.

[c13] The DRAM of claim 11 wherein said circuit operable to generate said interlock signal includes a sample bitline

and is operable to generate said interlock signal in response to a change in a voltage of said sample bitline

[c14] The DRAM of claim 12 wherein said sample bitline is a sample read bitline coupled to a plurality of gain cells of said array of gain cells and coupled to a sample sense amplifier.

[c15] The DRAM of claim 14 wherein said circuit operable to generate said interlock signal includes a differential amplifier coupled to said sample bitline to receive a first input voltage and coupled to receive a reference voltage as a second input voltage, said differential amplifier being operable to generate said interlock signal when said first input voltage crosses a level of said reference voltage.

[c16] The DRAM of claim 15 wherein said reference voltage has a programmably adjustable value.

[c17] The DRAM of claim 15 wherein said differential amplifier includes a first transistor having a gate coupled to said sample bitline to receive said first input voltage and a second transistor having a gate coupled to said reference voltage as said second input voltage, wherein said circuit is operable to generate said interlock signal as a voltage on at least one of a source and a drain of said second transistor, wherein a size of said gate of said first tran-

sistor is larger than a size of said gate of said second transistor such that a voltage gain of said second transistor is larger than a voltage gain of said first transistor.

[c18] The DRAM of claim 17 wherein said differential amplifier further includes a pair of transistors each having gates coupled to a common input potential and at least one of a source and a drain coupled to a common supply potential

[c19] The DRAM of claim 13 wherein said DRAM further comprises means for timing the setting of a sense amplifier in relation to said interlock signal.

[c20] The DRAM of claim 13 wherein said DRAM further comprises means for timing the precharging of read bitlines of said array of gain cells in relation to said interlock signal.